IN THE CLAIMS:

Please amend the claims as follows:

1. (Withdrawn) Method for measuring the delay time of at least one signal line connecting a memory buffer with a memory module comprising the following steps:

(a) sending a measurement start command from said memory buffer to said memory module and simultaneously starting an integration circuit provided within said memory buffer;

(b) transmitting a measurement pulse via said signal line; and

(c) stopping the integration circuit when the measurement pulse transmitted via said signal line is detected by a pulse detector provided within said memory buffer, wherein the integrated value of the integration circuit indicates the delay time of said signal line.

2. (Withdrawn) The method according to claim 1, wherein a measurement pulse generator provided within said memory module is activated after reception of the measurement start command by said memory module to transmit a measurement pulse via said signal line to said memory buffer.

3. (Withdrawn) The method according to claim 1, wherein a measurement pulse generator provided within said memory buffer is activated simultaneously with the integration circuit when the measurement start command is sent to said memory module to transmit a measurement pulse via said signal line to said memory module.

4. (Withdrawn) The method according to claim 3, wherein the memory module retransmits the measurement pulse received via said signal line back to the memory buffer when the memory module has received the measurement start command.

5. (Withdrawn) The method according to claim 1, wherein the measurement start command is sent from said memory buffer to said memory modules via a control line of a command and address bus.

6. (Withdrawn) The method according to claim 2, wherein the measurement pulse generator is clocked by a clock signal having a predetermined clock period.

7. (Withdrawn) The method according to claim 6, wherein the integration circuit is supplied with a phase adjusted clock signal to integrate time fractions of the clock period of said clock signal to the delay time of said signal line.

8. (Withdrawn) The method according to claim 7, wherein the clock signal is generated by a clock signal generator.

9. (Withdrawn) The method according to claim 1, wherein the measured delay time of said signal line is stored in a signal line delay memory provided within said memory buffer.

10. (Withdrawn) The method according to claim 9, wherein a delay time compensation unit provided within said memory buffer is adjusted depending on the delay time which is stored in said signal line memory such that all signal lines connecting said memory buffer to different memory modules comprise an equal standard time delay.

11. (Withdrawn) The method according to claim 1, wherein the signal line is a data line of a bi-directional data bus.

12. (Withdrawn) The method according to claim 1, wherein the measurement start command is generated by a control logic of said memory buffer.

13. (Previously Presented) A memory buffer for a memory module board which is connected via a signal line to a plurality of memory modules mounted on said memory module board having different signal line lengths, wherein the memory buffer comprises for each signal line a corresponding integration circuit for integrating the transmission time of a measurement pulse transmitted via said signal

line between said memory buffer and a memory module connected to said signal line.

14. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer comprises a control logic which sends a measurement start command to the memory modules via a control line of a command and address bus.

15. (Previously Presented) The memory buffer according to claim 13, wherein the signal line is a data line of a bi-directional data bus.

16. (Previously Presented) The memory buffer according to claim 13, wherein each integration circuit is connected to the control logic to receive a start signal when the measurement start command is sent to the memory modules.

17. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer comprises a measurement pulse detector which detects a measurement pulse received via said signal line.

18. (Previously Presented) The memory buffer according to claim 13, wherein the integration circuit of a signal line is connected to a corresponding measurement pulse detector of said signal line to receive a stop signal when a measurement pulse is detected by said pulse detector.

19. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer comprises a signal line delay memory for storing the integrated values of all integration circuits provided within said memory buffer as delay times of the corresponding signal lines.

20. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer (1) comprises a delay compensation unit which compensates the delay times of the signal lines depending on the delay times stored in said signal line

delay memory to provide an equal standard time delay for all signal lines of said memory buffer.

21. (Previously Presented) The memory buffer according to claim 13, wherein the integration circuits are supplied with a phase adjusted clock signal generated by a clock phase generator to integrate time fractions of a clock period of a clock signal generated by a clock signal generator provided within said memory buffer.

22. (Previously Presented) The memory buffer according to claim 13, wherein the memory buffer comprises a measurement pulse generator which transmits a measurement pulse via the signal line when the control logic sends a measurement start command to the memory modules .

23. (Previously Presented) The memory buffer according to claim 13, wherein the delay compensation unit is connected via signal lines to a microcontroller mounted on a motherboard.

24. (Previously Presented) The memory buffer according to claim 13, wherein the memory modules are DRAMs.